CALIFORNIA STATE UNIVERSITY LONG BEACH

DEPARTMENT OF ELECTRICAL ENGINEERING

EE.470 – DIGITAL CONTROL SYSTEMS –Spring 2010

Instructors: Dr. B. Shahian and Prof. Gary Hill

PROJECT #1

Submitted by:
Scott Thompson, 006001526

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Contents

Introduction

This project aims to model a satellite as a double integrator in the analog domain using op-amps. Since this "plant" is inherently unstable, we start our design by including an analog lead compensator (similar to a proportional/derivative controller) as well as an adjustable gain that will adjust the damping ratio of the system. With the proper selection of gain values, we can adjust the system response to be very slow (overdamped) or very fast (underdamped). As we explore a lower damping ratio, we begin to see overshoot and ringing before the system finally settles on the steady-state value. A fixed value is simulated using the Simulink package available in MATLAB and compared with the analog system.

Plant Design

Ideally, the plant transfer function is to be $1/s^2$, but due to input offset currents and voltages of the op-amps (any practical device), a Miller (lossy) integrator was designed to provide a DC feedback path.

The plant transfer function of a single integrator is given by:

$$G(s) = \frac{-1}{R_i C_f \left(s + \frac{1}{R_f C_f} \right)}$$

Recall that we will be putting two of these integrators in series, giving our total plant transfer function as:

$$G\ s\ = \frac{1}{R_{i1} C_{f1} R_{i2} C_{f2} \left(s + \frac{1}{R_{f1} C_{f1}} \right) \left(s + \frac{1}{R_{f2} C_{f2}} \right)}$$

To closely match our desired plant transfer function of $1/s^2$, we allow for the following conditions:

$$R_i C_f = 1$$
$$R_f C_f \gg 1$$

We have a number of options in the choice of normalizing *R* and *C*, but typically large-valued electrolytic capacitors have (1) high leakage currents which lead to saturation of the op-amp, and (2) have very loose tolerances. We chose polyester, Mylar, ceramic, or polypropylene capacitors due to their tighter tolerances, but such choices leaves us with relatively small capacitance values (typically less than 1 µF). Since the product of *RC* must equal one for our design, one value is inversely proportional to the other. A very small value of *C* will result in a very large value for *R*. Depending on the op-amp chosen and the noise constraints, input offset currents can also cause undesirable DC effects on the system.

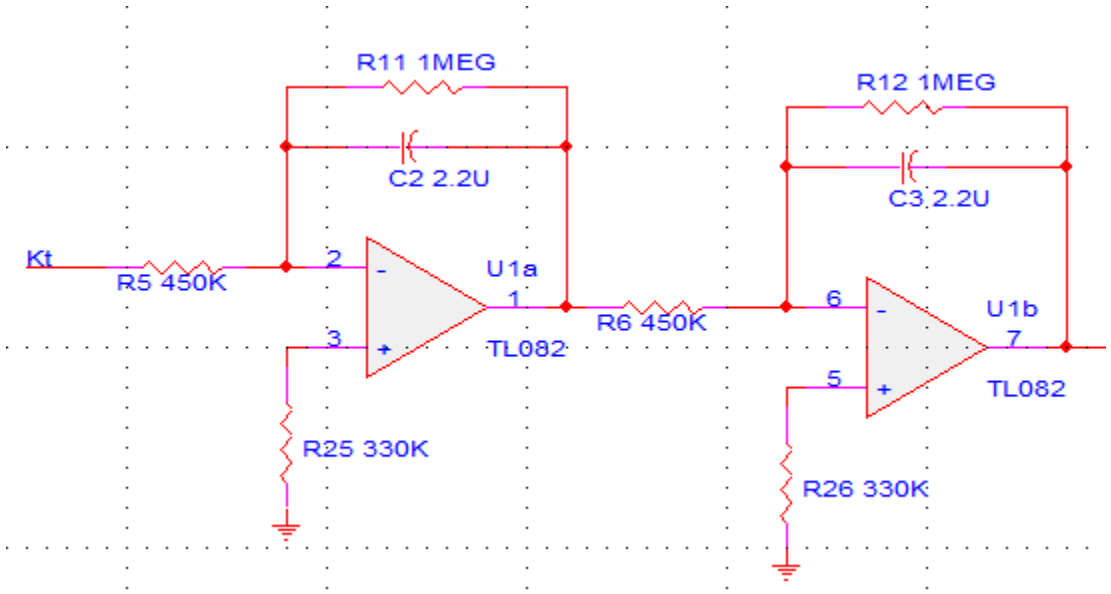
Using an on-hand Mylar capacitor of 1 µF, a standard resistor value of 1 MΩ is a moderate upper-limit for a mid-range op-amp with good DC performance and drift characteristics. However, a search of the local electronics shop had a special buy for some 2.2 µF capacitors. This necessitated a change in the input resistor value to 454.55 kΩ. To reach a close approximation of this, two standard on-hand resistor values of 1 MΩ and 820 kΩ were placed in parallel to yield a resistance of 450.55 kΩ (an error of -0.9%).

I used a 1 MΩ resistor for the feedback resistor. Ideally, this should be as large as possible (up to about 10 MΩ). The small error in the transfer function is an exponential term with a time constant of 2.2 s.

Op-Amp Selection

From my experience in low-frequency DC op-amp circuitry, I would normally use an OP-27EP op-amp due to its excellent stability, noise, and offset characteristics. However, due to the number of devices needed for this design and given the loose layout on the breadboard (that would mitigate the necessity of the low offset due to the relatively high impedance of the ground plane), a general-purpose FET-input op-amp (TL082 dual, or TL084 quad) was used.

Plant Circuit



Compensator Design

Looking in my prior EE.370 textbook, *Design of Feedback Control Systems, 4th ed.*, by Stefani, Shahian, Savant, and Hostetter, I see the desired circuit for a lead compensator given our in-class transfer function requirement of:

$$K\ \ s\ \ = k\frac{s+1}{s+10}$$

Here, *k* is a gain coefficient that will likely be included in a pre-stage gain block. In the book, this transfer function appears as the following sets of equations and values (figure 1.14e, p23):

$$\frac{k(s+b)}{s+a}$$

$$\begin{aligned} k &= R_f \,/\, R_1 \\ b &= 1 \,/\, R_2 C_1 \\ a &= (1 + R_2 \,/\, R_1) b \end{aligned}$$

If we temporarily neglect a value for *k*, we know that $b = 1$ and $a = 10$ from our desired compensator transfer function. From similar design goals when picking values for our integrator stage, we will solve the "*b*" equation, giving $R_2 = 1\ \mathrm{M\Omega}$ and $C_1 = 1\ \mu\mathrm{F}$.

Now we can focus on solving the "*a*" equation, as shown in the following steps:

$$\begin{aligned} 10 &= 1 + 10^6 \,/\, R_1 \\ 9 &= 10^6 \,/\, R_1 \\ R_1 &= 10^6 \,/\, 9 \cong 111.11\ \mathrm{k\Omega} \end{aligned}$$

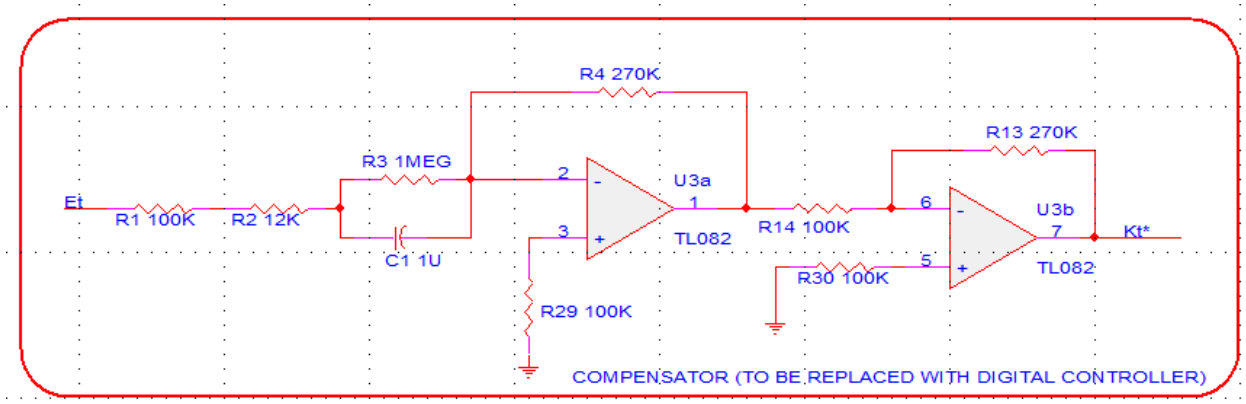
To "fine tune" this compensator circuit, we can create an equivalent resistor by using a standard value of, say, 100 kΩ in series with an adjustable 25 kΩ potentiometer. However, it is quite a bit cheaper to use a standard value of 12 kΩ to give a value of 112 kΩ. This error is:

$$\left(\frac{112}{111.11} - 1\right) \times 100\% = 0.8\%$$

We can adjust the value of the feedback resistor to give us a desired gain by using a potentiometer, or we can arbitrarily pick a fixed value and compensate for its effect by adjusting the gain in a prior (or following) stage. Due to the rather large resistances considered, it is likely better to add a gain stage with lower-valued resistors that can be used to adjust our overall system gain as well as compensate for any value mismatches in the plant's transfer function components. For convenience in setting the various gains and allowing for possible level shifting when going into the digital domain, I chose to add a second inverting gain stage. The overall gain of the compensator circuit (to prevent saturation of this stage) is:

$$k = \left(\frac{270}{112}\right)\left(\frac{270}{100}\right) \cong 6.5$$

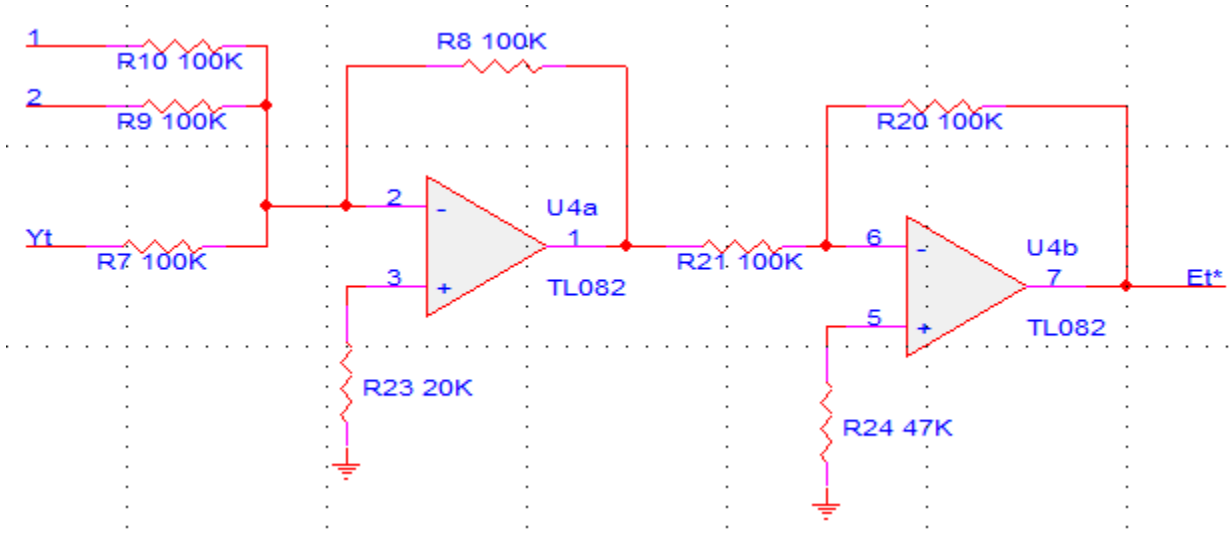
Compensator Circuit



Summing Junction Design

The summing junction is simply an active inverting summer using op-amps. Due to the resulting "sign" of the forward transfer function, the inverting input was available to be used for both the input step function as well as the feedback path. Again, for convenience in setting gains and to allow for future expansion, a second op-amp (part of the same package) was used to restore the original polarity of the input error.

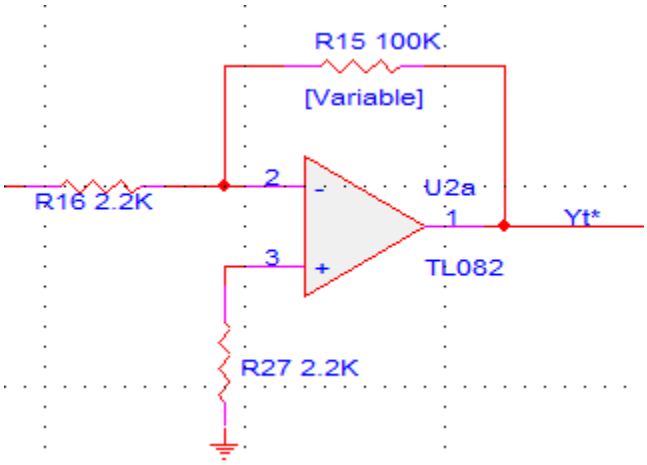
Summing Junction Circuit



Integration Gain Stage, ADC Bias, and Level Shifter

An additional gain stage was added after the second integrator to maximize the dynamic range of the system without saturation. If all of the gain were placed in prior stages (e.g., the error amplifier or compensator circuit), those stages would tend to saturate when attempting to achieve an overall gain suitable for a fast system response. Also, since the output of the analog plant was to be digitally sampled with a unipolar analog-to-digital converter (ADC) on-board the microcontroller, additional stages provided gain and level shifting, as summarized below.

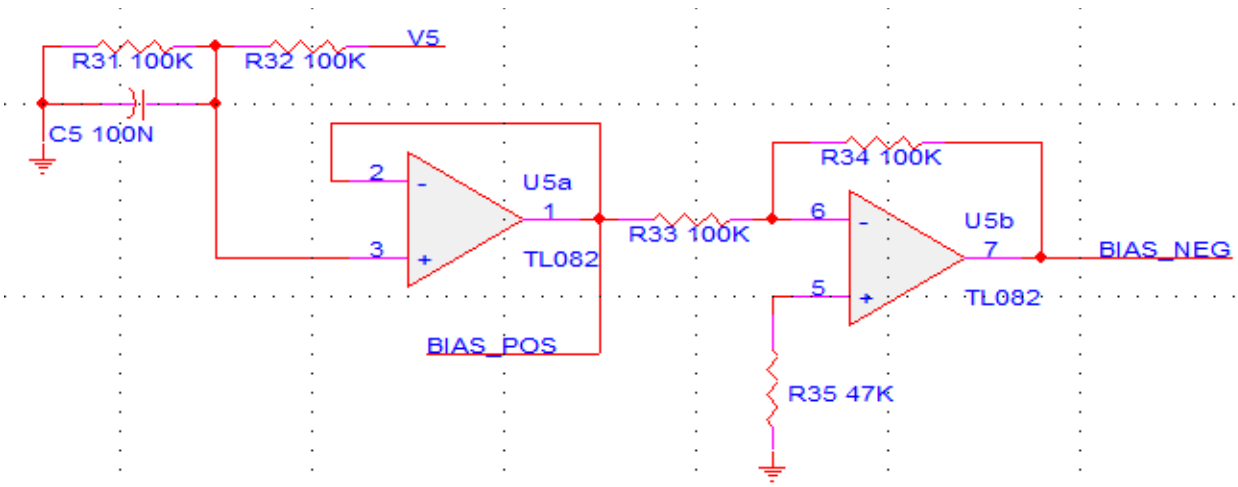
Integrator Gain Stage Circuit



Here, we have a gain of about 45, taken from the output of the second integrator and being fed back to the input summing junction.

ADC Bias Generator

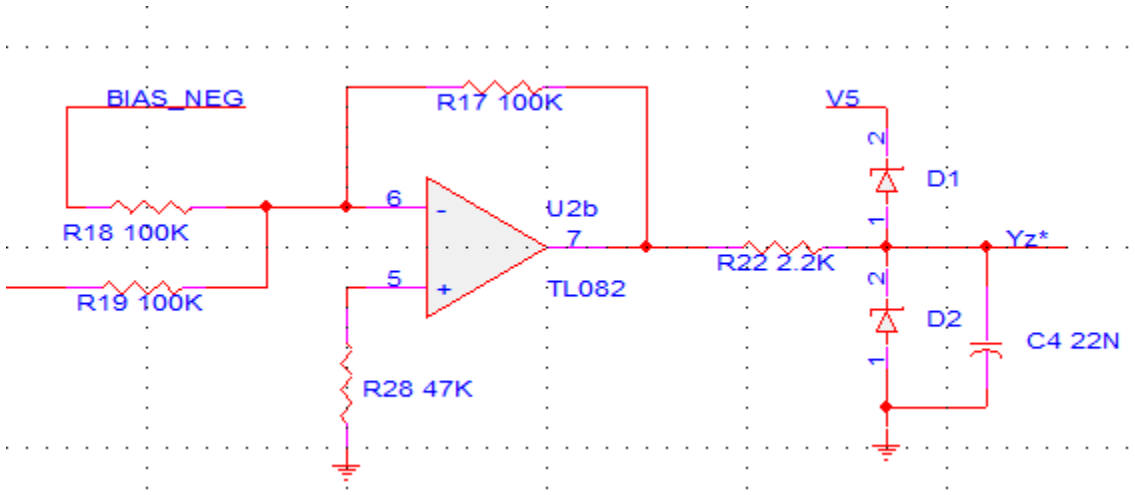
Since I was operating from a regulated +5 V power supply and achieved my op-amp supply voltages from a DC-DC converter, I split the +5 V rail to create an offset of ±2.5 V, shown in the following circuit.



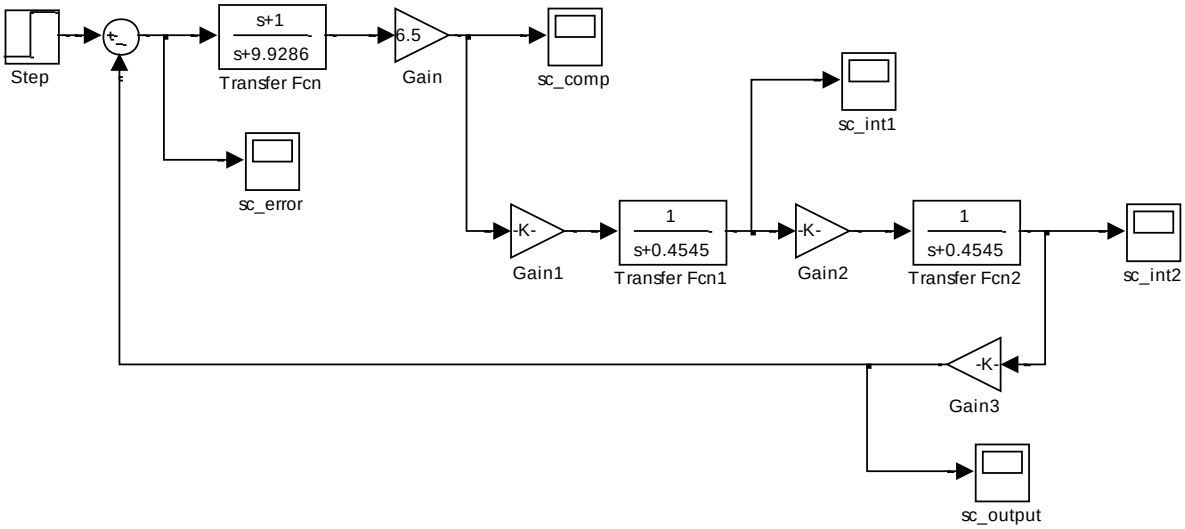
Level Shifter and Clamping

Finally, the output of the preceding integrator gain stage is fed to another inverting summer, with one input to the summer being a constant DC voltage of -2.5 V. This produces a shift from the 0 V level to +2.5 V. Given the 0 V to 5 V range of the MCU's ADC, we effectively have an allowable bipolar range of ±2.5 V centered on the +2.5 V bias. The output resistor is in place to limit the current through the op-amp as well as the clamping diodes and the MCU in the event of the op-amp's output voltage going below 0 V or above +5 V. Although the MCU likely has protection diodes at each input (making D1 and D2 redundant), it is still paramount to use the current-limiting resistor (R22 in this design) to prevent damage to the expensive MCU.

Level Shifter and Clamping Circuit

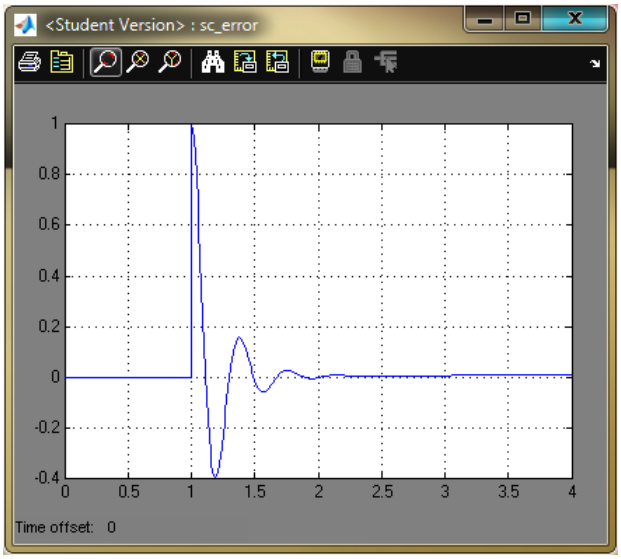


Simulink Circuit

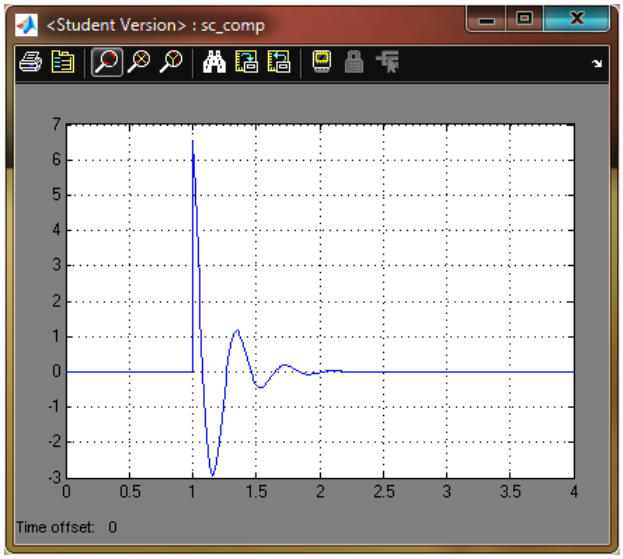


Simulink Plots

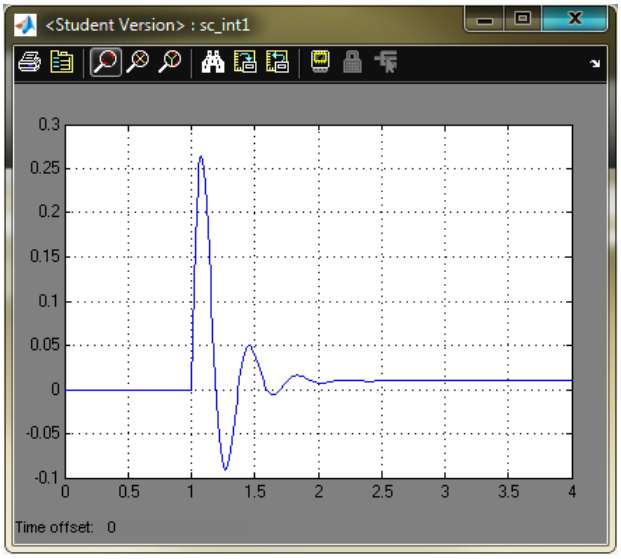
The following plots are listed to show the output of each stage that would be implemented with op-amps. This data is used to verify that we will not saturate with ±15 V rails.



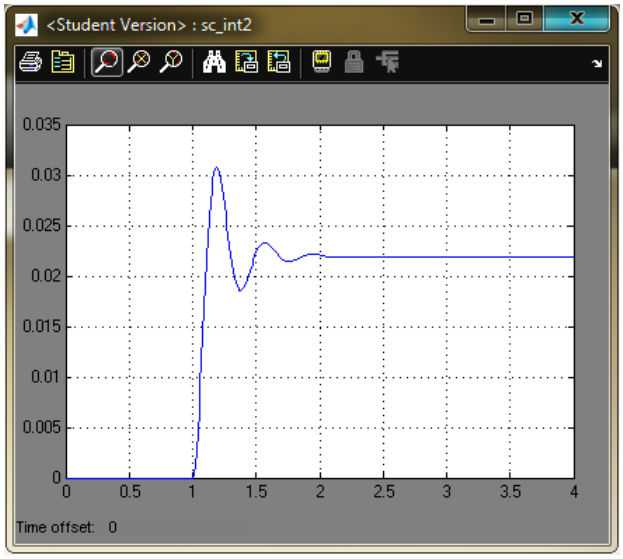
Output of the Error Amplifier



Output of the compensator



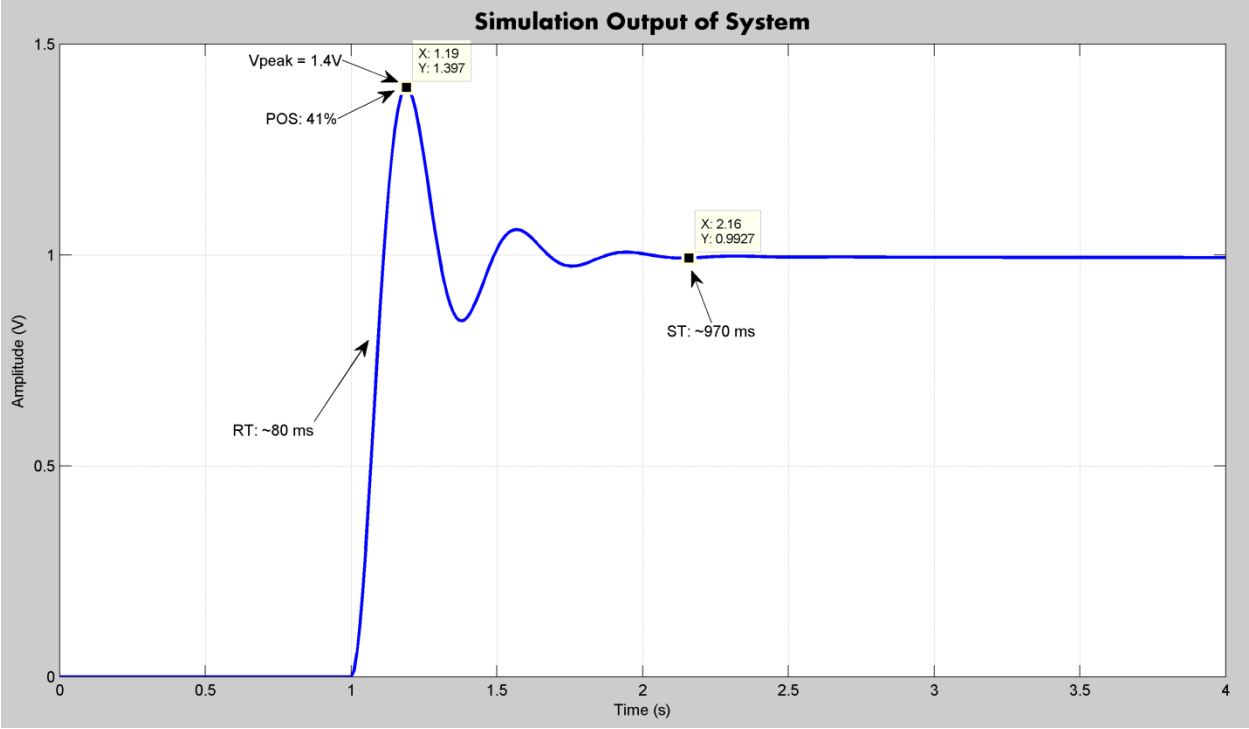
Output of Integrator #1



Output of Integrator #2

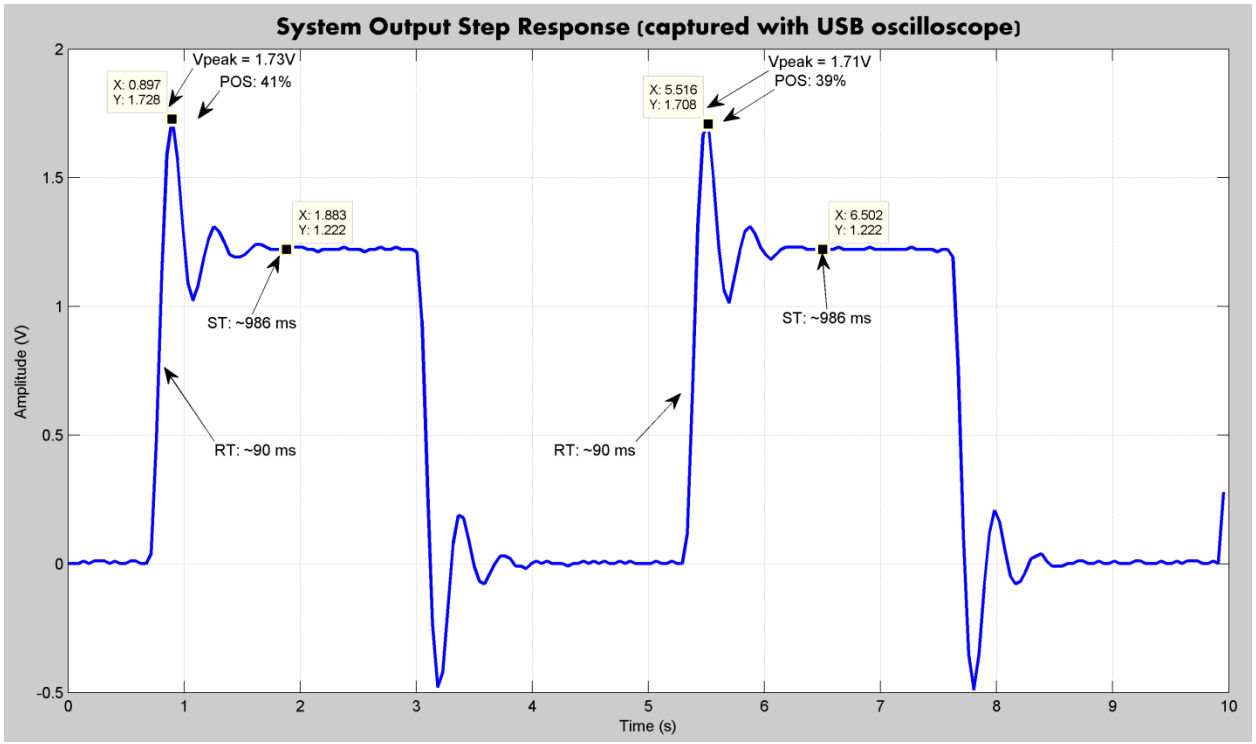
Output of Simulation

The final output from our simulated system is shown in the following figure for a 1 V step input. When we make our comparisons with the results from the full analog system, we will scale the amplitudes so that they are normalized.



Hardware Output (via USB Oscilloscope)

A 10-bit USB-powered oscilloscope from Parallax (PropScope) was used to digitize a 10-second window of the analog system. The step input was provided via a voltage divider from the output of a slow timer on the dsPIC MCU board. The "damping ratio" potentiometer was set to approximately one-half of its nominal 200 kΩ value, or about 100 kΩ—the value used in the simulation. This will allow us to compare the two results and draw a conclusion from the error analysis. The 'scope data was saved as a comma separated value (CSV) format and imported into MATLAB for quick plotting. The data tip cursor was used to locate the various locations on the plot in order to calculate the required parameters. This figure is given below.



Comparison of Theoretical vs. Actual Data

By visual inspection, we see that the output has a similar shape and "feel" to the simulated version of our system. Also, probing the various analog outputs shows similar compatibilities with the simulated response. Moreover, nonlinearities due to op-amp saturation, in particular, are not observed with a bounded step input.

The analog circuit provided a 1.25 V nominal step to facilitate the maximization of the dynamic range in the A/D converter on the dsPIC MCU. Recall that we have allowed for a ±2.5 V swing that is centered on a +2.5 V offset, giving a 0 V to 5 V input to the A/D converter. To allow for the overshoot and undershoot of the circuit, we had to lower the input step voltage. Our steady-state input maximum can be found by manipulating the equation for the percent overshoot.

$$POS = \left(\frac{V_{peak}}{V_{ss}} - 1 \right) \cdot 100\%$$

$$V_{peak} = V_{ss} \left(\frac{POS}{100\%} \right) + 1$$

$$V_{ss} = \frac{V_{peak}}{POS \,/\, 100\% + 1}$$

On the extreme end with a 0% POS, $V_{ss} = V_{peak} = 2.5 \text{ V}$. To allow for a 100% POS, we see that $V_{ss} = V_{peak} \,/\, 2 = 1.25 \text{ V}$, which is what our design allows (in theory).

Two values from the simulation data need to be normalized before direct comparison can be made to the analog system. These values are the peak voltage and the steady-state voltage. Other measurements are either taken on the horizontal (time) scale, or are otherwise unchanged from the scaling (e.g., the rise-time calculation).

$$V_{peak,sim} = 1.397\ \text{V}\left(\frac{1.222\ \text{V}}{0.993\ \text{V}}\right) = 1.72\ \text{V}$$
$$V_{ss,sim} = 0.993\ \text{V}\left(\frac{1.222\ \text{V}}{0.993\ \text{V}}\right) = 1.22\ \text{V}$$

We will average the two values shown on the analog system's output to yield a representative value for comparison. The rise time and settling time values are the same for both readings, so they will be used as-is.

$$V_{peak,ave} = \left(\frac{1.73\ \text{V} + 1.71\ \text{V}}{2}\right) = 1.72\ \text{V}$$
$$POS_{ave} = \left(\frac{41\% + 39\%}{2}\right) = 40\%$$

Percentage errors (relative to the simulation data) for the peak voltage, steady-state voltage, and percent overshoot (POS) are:

$$\%err_{Vpeak} = \left(\frac{1.72\ \text{V}}{1.72\ \text{V}} - 1\right)\cdot 100\% = 0\%$$
$$\%err_{Vss} = \left(\frac{1.22\ \text{V}}{1.22\ \text{V}} - 1\right)\cdot 100\% = 0\%$$
$$\%err_{POS} = \left(\frac{40\%}{41\%} - 1\right)\cdot 100\% = -2\%$$

Percentage errors (relative to the simulation data) for the rise time and settling time are:

$$\%err_{RT} = \left(\frac{90\ \text{ms}}{80\ \text{ms}} - 1\right)\cdot 100\% = 13\%$$
$$\%err_{ST} = \left(\frac{986\ \text{ms}}{970\ \text{ms}} - 1\right)\cdot 100\% = 2\%$$

All errors between the simulated data and the actual, measured, data are extremely small—except for the error in the rise time calculation. We note that this error is large due to the large jumps in the output amplitude versus the moderate time increment. Due to the very slow nature of the input signal, finding the 10% and 90% levels was impossible using the data cursor function of MATLAB. It is expected that the actual error will fall in line with the lower errors given for the rest of the system.

Conclusion

An analog system, consisting of a plant, compensator, and gain, was implemented using operational amplifiers on a standard prototyping breadboard. Power was supplied via a +5 VDC regulated supply, and the elevated op-amp supply was provided by a small 1.5 W DC-DC converter. For convenience in setting the system's gain as well as allowing for possible level shifting for future labs (where the compensator will be implemented in the digital domain on a microcontroller), additional gain stages were placed between each major block. The gain stage at the output of the second integrator was allowed to vary with a potentiometer and provided the adjustment needed of the damping ratio. A fixed gain value was chosen and the system was simulated and plotted using Simulink and MATLAB. To facilitate comparison and plotting, the analog system was digitized with a Parallax, Inc. "PropScope" USB oscilloscope and plotted in MATLAB. The theoretical (simulation) values were compared with the actual measured values and found to be extremely close (typically within 2%). The only exception was the comparison of the rise time, but the discrepancy is well accounted for by noting that the slope was too steep given the relatively long sample time. This made it impossible to use the raw data to determine the exact 10% and 90% locations for the required calculations. Visually, the graphs were very similar and this anomaly was mitigated and accepted to be well within specifications.

Appendix A: Schematic Diagram (PSPICE Version)

The following page has the PSPICE schematic of the analog system. Not shown is the dsPIC microcontroller, DC-DC converter, and power supply decoupling capacitors, etc.