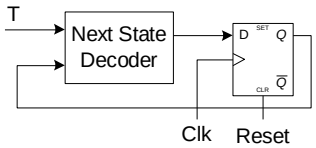
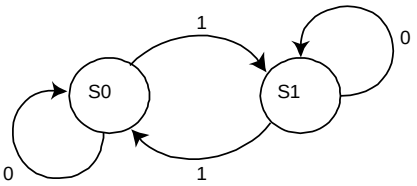
Hill
EE 201
11/30/11

Homework #5

1. Using sequential circuit design procedure beginning with a state diagram, convert a D-type flip-flop to a T-type flip-flop by adding input logic. Show that the logic obtained is an exclusive-OR gate..



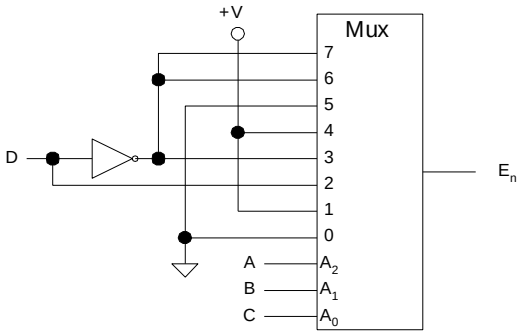
Present State	Inputs	Next State
Q(t)	*T*	*D(t)*
0	0	0
0	1	1
1	0	1
1	1	0



$D = \overline{Q} \cdot T + Q \cdot \overline{T}$ This is the definition of an exclusive or gate!

2. Implement the following Boolean function with an 8-to-1 line multiplexer and a single inverter:
$F(A,B,C,D) = \sum m(2,3,5,6,8,9,12,14)$

A	**B**	**C**	**D**	**F**	
0	0	0	0	0	*F=0*
0	0	0	1	0	
0	0	1	0	1	*F=1*
0	0	1	1	1	
0	1	0	0	0	*F=D*
0	1	0	1	1	
0	1	1	0	1	$F = \overline{D}$
0	1	1	1	0	
1	0	0	0	1	*F=1*
1	0	0	1	1	
1	0	1	0	0	*F=0*
1	0	1	1	0	
1	1	0	0	1	$F = \overline{D}$
1	1	0	1	0	
1	1	1	0	1	$F = \overline{D}$
1	1	1	1	0	



3. Design a sequential circuit using two D flip-flops A and B and combinational logic. Your circuit has one input X and one output Y, and is defined by the following state diagram — Traditional Design Solution

Present State		Inputs	Next State		Output
$Q_1(t)$	$Q_0(t)$	X	$D_0(t)$	$D_0(t)$	Y
0	0	0	0	1	1
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	1	1	0
1	0	0	1	0	0
1	0	1	0	0	0
1	1	0	1	0	0
1	1	1	1	1	0

D_1

Q_1 \ Q_0X	00	01	11	10
0			1	
1	1		1	1

$D_1 = Q_0X + Q_1\overline{X}$

D_0

Q_1 \ Q_0X	00	01	11	10
0	1		1	1
1			1	

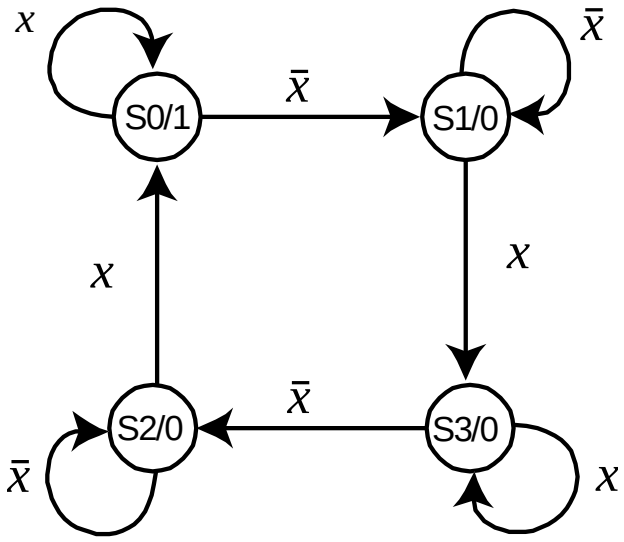
$D_0 = Q_0 \cdot X + \overline{Q_1} \cdot \overline{X}$

Y

Q_1 \ Q_0X	00	01	11	10
0	1	1		
1				

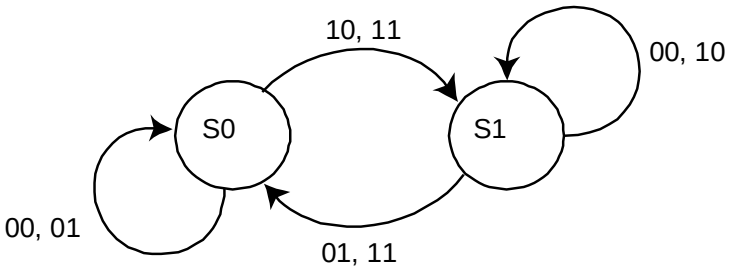
$Y = \overline{Q_1} \cdot \overline{Q_0}$

4. A sequential circuit has two flip-flops A and B, one input X and one output Y. The state diagram is shown below. Design the circuit with D flip-flops. — Design using One-Hot State Encoding



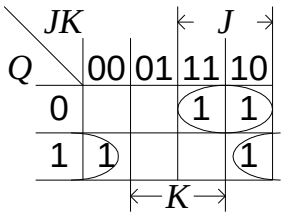
$$S0(t+1) = D0(t) = X \cdot S0 + X \cdot S2 = X(Q0 + Q2)$$
$$S1(t+1) = D1(t) = \overline{X} \cdot S0 + \overline{X} \cdot S1 = \overline{X}(Q0 + Q1)$$
$$S2(t+1) = D2(t) = \overline{X} \cdot S2 + \overline{X} \cdot S3 = \overline{X}(Q2 + Q3)$$
$$S3(t+1) = D3(t) = X \cdot S1 + X \cdot S3 = X(Q1 + Q3)$$
$$Y(t) = S0(t) = Q0$$

5. Convert a D-type flip-flop into a JK flip-flop, using external gates. The gates can be derived by means of a sequential circuit design procedure starting from a state table with the D flip-flop output as the present state and its input as the next state and with J and K as circuit inputs.



Present State	Inputs		Next State
Q(t)	*J*	*K*	*D(t)*
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

D



$$D = \overline{Q}J + Q\overline{K}$$