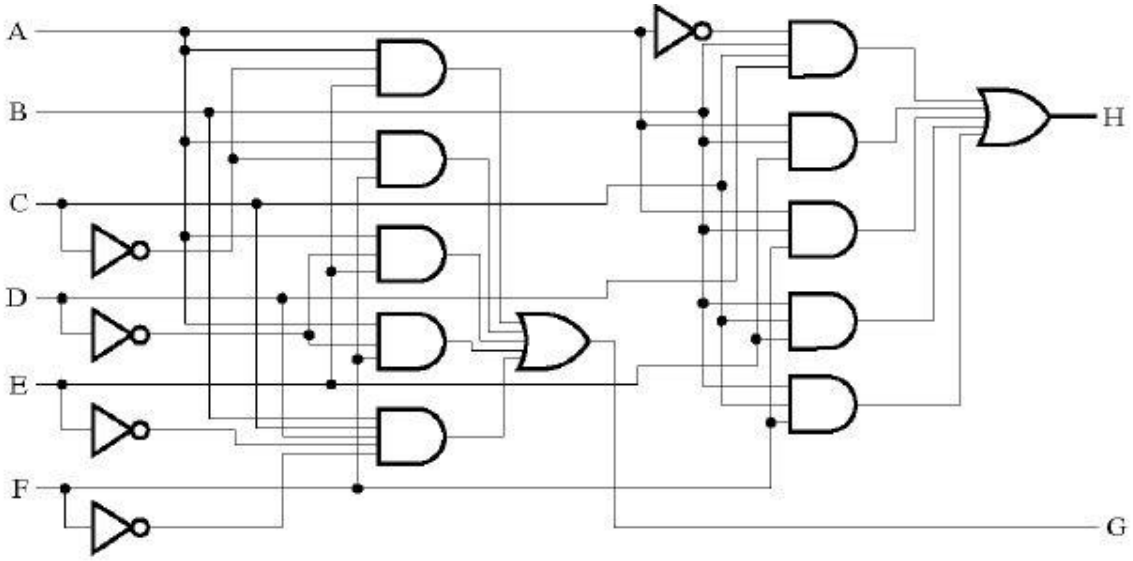
Hill
EE 201
11/20/2011

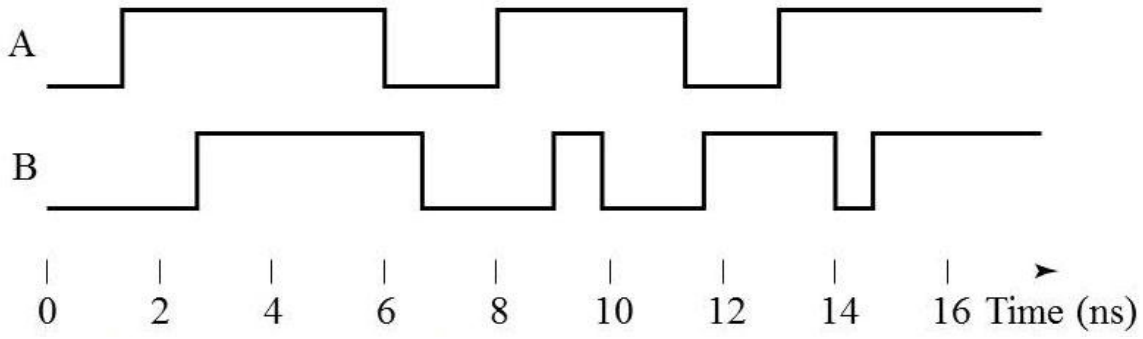
# Homework #4

1. An integrated circuit logic family has NAND gates with a fan-out of 8 standard loads and buffers with a fan-out of 16 standard loads. Show how the output signal of a single NAND gate can be applied to 38 other gate inputs using buffers. Assume that each input is one standard load.

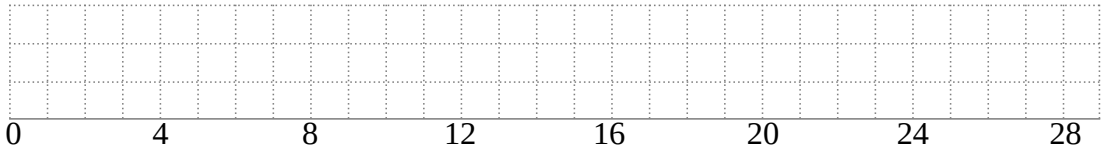
2. The gates including inverters in the figure below have propagation delays of $t_{pd} = 0.5$ ns. What is the propagation delay of the longest path through the circuit?



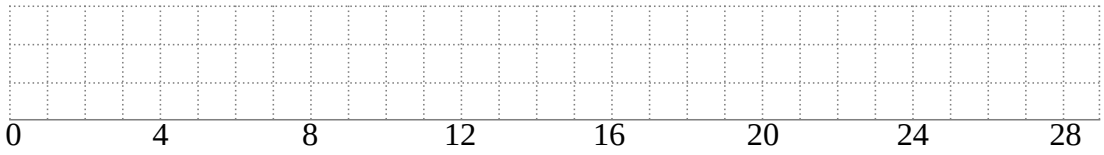

**3.** The waveform in the figure below is applied to an AND gate. Find the output of the AND assuming that:



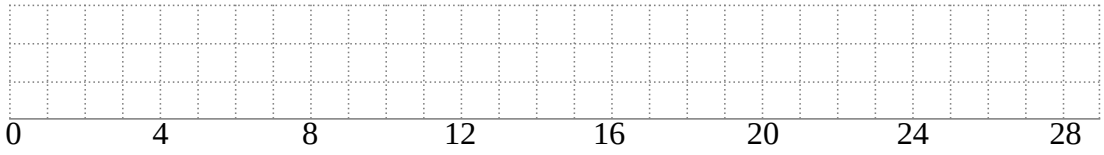

(a) it has no delay.



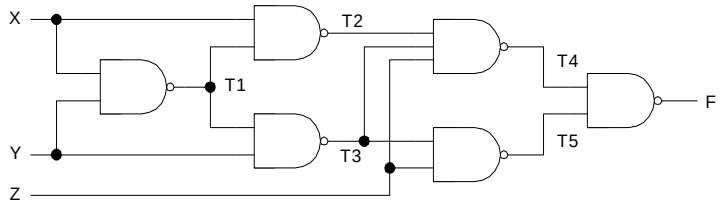

(b) it has a transport delay of 2 ns.




(c) it has an inertial delay of 2 ns with a rejection time of 1 ns.

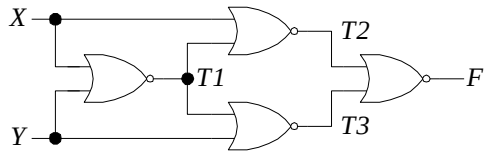



4. (a) Obtain the truth table for the circuit shown below. (b) Draw an equivalent circuit for F with fewer NAND gates.




| *X* | *Y* | *Z* | *T1* | *T2* | *T3* | *T4* | *T5* | *F* |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | | | | | | |
| 0 | 0 | 1 | | | | | | |
| 0 | 1 | 0 | | | | | | |
| 0 | 1 | 1 | | | | | | |
| 1 | 0 | 0 | | | | | | |
| 1 | 0 | 1 | | | | | | |
| 1 | 1 | 0 | | | | | | |
| 1 | 1 | 1 | | | | | | |

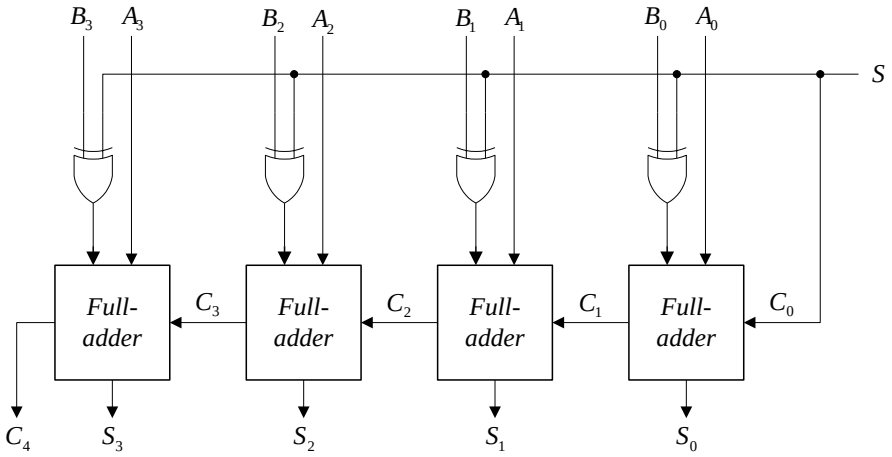
5. By using Boolean algebra, verify that the circuit shown generates the exclusive-NOR function




6. Lookup the logic diagram for a 74HC138 MSI CMOS circuit on the web. (a) Write the Boolean function for each of the outputs. (b) Describe carefully the circuit function.

7. Design a combinational circuit that detects an error in the representation of a decimal digit in BCD. In other words, obtain a logic diagram whose output is equal to 1 when the inputs contain any one of the six unused bit combinations in the BCD code.

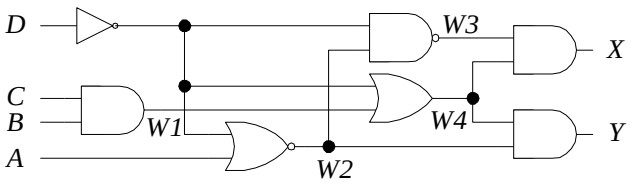
8. The adder-subtractor circuit shown below has the following values for input operation S and data inputs A and B. Determine, in each case, the values of the outputs $S_3$, $S_2$, $S_1$, $S_0$ and $C_4$.




The state of S, as illustrated by the circuit, determines if B is added to or subtracted from A. All subtractions use 2's complement arithmetic $S = A + (\overline{B} + 1)$.

| | **S** | **A** | **B** | **$C_4$** | **$S_3$, $S_2$, $S_1$, $S_0$** |
|---|---|---|---|---|---|
| (a) | 0 | 0111 | 0100 | | |
| (b) | 0 | 0100 | 0111 | | |
| (c) | 1 | 1101 | 1010 | | |
| (d) | 1 | 0101 | 1010 | | |
| (e) | 1 | 0000 | 0011 | | |

9. (a) For the circuit shown complete the truth table. (b) Draw a simplified 2-level SOP circuit which is equivalent to the circuit and its corresponding truth table.




**Truth Table**

| A | B | C | D | W1 | W2 | W3 | W4 | X | Y |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | | | | | | |
| 0 | 0 | 0 | 1 | | | | | | |
| 0 | 0 | 1 | 0 | | | | | | |
| 0 | 0 | 1 | 1 | | | | | | |
| 0 | 1 | 0 | 0 | | | | | | |
| 0 | 1 | 0 | 1 | | | | | | |
| 0 | 1 | 1 | 0 | | | | | | |
| 0 | 1 | 1 | 1 | | | | | | |
| 1 | 0 | 0 | 0 | | | | | | |
| 1 | 0 | 0 | 1 | | | | | | |
| 1 | 0 | 1 | 0 | | | | | | |
| 1 | 0 | 1 | 1 | | | | | | |
| 1 | 1 | 0 | 0 | | | | | | |
| 1 | 1 | 0 | 1 | | | | | | |
| 1 | 1 | 1 | 0 | | | | | | |
| 1 | 1 | 1 | 1 | | | | | | |